E2SWITCH
Energy Efficient Tunnel FET Switches and Circuits

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E^2-SWITCH is reporting a significant progress in year 1 in all the technical work packages but also in terms of dissemination. The detailed status of the work in various work packages is summarized below while some other main activities are available on the project website: http://www.e2switch.org/ **or have been reported in our recent workshop *In the Quest of Zero Power: Energy Efficient Computing Devices and Circuits*, organized as a satellite event to ESSDERC/ESSCIRC 2014:**

(http://www.essderc2014.org/en/sistemacongressi/european-solid-state-device-conference-2014/website/home/**).**

The project press release is available here:
http://actu.epfl.ch/news/ultra-low-consumption-for-the-future-of-electron-2/

WP1 (leader: JUELICH)

JUELICH has developed and fabricated complementary gate-all-around Si nanowire TFETs using dopant segregation from silicide contacts to achieve steep doping profiles at the tunneling junction. Heterostructure TFETs with SiGe source and Si channel/drain provide reduced ambipolarity, and utilization of line tunneling increases the on-current. A novel SiGeSn heterostructure TFET has been conceived and corresponding epitaxial layer structures have been grown with high quality.

IBM has developed a technique to epitaxially grow high-quality III-V materials on Si substrates, inside oxide nanotube templates that determine the shape of the grown material. This break-through technology for the first time allows for III-V materials integration with standard Si(100) substrates at a level of control, uniformity and quality which is unprecedented. Using this approach, III-V heterostructures are being developed for all-III-V tunnel FETs that could give high performance, while also being compatible with standard semiconductor manufacturing processes.

Vertical transistors with a gate-all-around (GAA) geometry using arrays of InAs/GaSb nanowires grown on Si substrates have been fabricated and electrically characterized at LUND. A technique to controllably reduce the InAs/GaSb nanowire diameter by digital etching has been developed which will allow excellent gate control in the GAA geometry and open the possibility for band line-up engineering through exploiting quantum confinement.

WP2 (leader: IBM)

In WP2 we focus on the detailed characterization and analysis of tunnel diodes and Tunnel FETs (TFETs) fabricated in WP1 to extract the device and performance parameters relevant to logic and RF applications. The activities included setting up new measurement techniques, characterizing device performance and applying special measurement techniques such as pulsed current-voltage characterization, noise measurements and investigations of the influence of strain and temperature on the material and device performance.

In particular, a time-resolved measurement technique was set up which is sufficiently sensitive to detect signals in the nA regime on a nanosecond time scale. The technique was tested with Si nanowire TFETs and resulted in a suppression of the trap-assisted tunneling in the subthreshold regime. In combination with temperature-dependent measurements the band-to-band tunneling regime was identified.

Furthermore, InAs/Si and InAs/GaSb nanowire TFETs with gate-all-around architecture were investigated. The performance of vertical InAs/Si TFETs based on individual nanowires was boosted by scaling the equivalent oxide thickness achieving on-currents of 50 µA/µm at VGS=VDS=|1V|.

In addition, a setup for noise characterisation of vertical InAs/GaSb nanowire TFETs has been established and first measurements have been performed.

Moreover, the influence of strain was investigated demonstrating highly strained Si nanowires with very high tensile strain values up to 2.2% achieving increased on-currents by enhanced mobility.

WP3 (leader: ETHZ)

Objectives of WP3 in the first year have been to calibrate three simulation tools for the hierarchical modelling of tunnel FETs (TFETs): the full-band and atomistic quantum transport simulator OMEN of ETHZ, the 30 band k•p quantum transport simulator of IUNET, and the commercial TCAD tool Sentaurus-Device from Synopsys. Furthermore, it was the goal to develop reliable tunneling models for Si/SiGe, all-III-V, and Si/III-V hetero-junction nanowire TFETs fabricated in WP1 as well as to provide the technology partners in E2SWITCH with optimal design guidelines. All these objectives have been achieved.

The nonlocal Empirical Pseudo-potential Method (EPM) was applied to generate band structure parameters for the calibration of the Kane model in Sentaurus-Device using the tool S-Band of Synopsys. This was done for the group-IV element alloys, Si, Ge, and Sn. The band structures of GeSn and SiGeSn were calculated by employing the Virtual Crystal Approximation. The standard k•p framework has been extended by IUNET-BO to take into account the effects of strain in homo- and hetero-junction TFETs. Any kind of strain, from uniaxial to biaxial, from tensile to compressive can be taken into account, and the effect of strain on the electronic and transport properties of TFETs can be investigated.

ETHZ performed 3D simulations of the Si0:5Ge0:5/Si hetero-structure TFET fabricated by FZJ with the device simulator Sentaurus-Device using band-to-band-tunneling (BTBT) parameters calibrated to EPM values. The simulated ID-VGS characteristics of the device are in good agreement with the experimental curves. IUNET-Udine could demonstrate similarly good agreement by 2D simulations with parameters of the BTBT model calibrated against 30 band k·p calculations.

3D simulations of the latest InAs/Si nanowire hetero TFETs from IBM with BTBT parameters extracted from EPM calculations were started by ETHZ. Important design parameters are oxide thickness, diameter, and doping of the nanowire. The approach embraced by IUNET-BO for the modelling of these devices is based on the k•p Hamiltonian model. The k•p Hamiltonian parameters for the most important III-V semiconductors and p-type Si have been included in the code.

The most significant results in WP3 are: (1) Calibrated BTBT parameters for homo- and hetero-TFETs made of SiGe, all-III-V, Si/SiGe, GeSn/SiGeSn, Si/InAs, and GaSb/InAs junctions based on nonlocal EPM and 30 band k•p calculations. (2) Assessment of strain effect on performance of various TFET structures using the EPM and k•p frameworks. (3) Simulation (3D and 2D) and deeper understanding of the Si0:5Ge0:5/Si hetero-structure TFET fabricated by FZJ. (4) Antecedent setup and simulations of GeSn/SiGeSn hetero-TFETs. Design guidelines for favorable compositions and strain made available to FZJ for future fabrication. (5) 3D simulations of the latest InAs/Si nanowire hetero TFETs from IBM and decision on design variations.

WP4 (leader: EPFL)

WP4 has achieved an excellent alignment of the reported results with the initial planning by a joint effort of EPFL, ETHZ IUNET-Udine and IUNET-Bologna. We have been able to setup and to validate a simulation platform for the Density-Of-States (DOS) switch and the dimensionality influence and importance.

The OMEN tool has been made available for the study of density-of-states (DOS) including1-D (bulk, 3D DOS), 2-D (quantum well, 2D DOS), and 3-D (nanowire, 1D DOS) structures, including band-to-band tunnelling along all the possible directions, and covering a wide range of materials and material combinations, quantum mechanical effects such as quantization and confinement

A new dedicated simulator tool was developed, relying on the 1-D self-consistent solution of Poisson and closed-boundary Schrodinger equations, taking into account nonparabolicity effects for both the subband energies and the WFs as well as the DoS and calculating BTBT current (both phonon-assisted and direct) as post-processing. Two direct tunnelling (Bardeen's transfer Hamiltonian and Kane's approach) models have been included.

Advanced simulations and optimization of EHBTFET have been performed and the origin of the leakage in this structure has been clarified. Two new device architectures have been proposed to address leakage.

Two device concepts highlighting the importance of the alignment between the electric field and the tunneling path have been proposed, investigated and experimentally proven, which is placing this work in advance compared to the initial planning.

First quantitative evaluations of the role of strain by SDevice and Multi-subband Monte Carlo simulations on template devices close to the silicon nanowires fabricated in the project are reported, demonstrating a strong link between this WP4 and WP1.

WP5 (leader: IMEC)

Mixed signal simulation deck has been developed to support mixed mode simulation of TFET circuit. The simulator has been calibrated based on standalone device and allows evaluating circuit architecture in DC and AC application. Thanks to this work, evaluation of key elementary circuit block will be performed, with reasonable accuracy, without having to rely complex processing.

Therefore new circuit architectures can be investigated before fabrication. This would enable to identify the most promising circuits, which would be fabricated later in the project.

In parallel with the improvement of the simulation capability, circuit architecture study for analog, focusing on sensor application, and logic, for scaled technologies, have been engaged in order to bring some application driven constrain. Bringing more circuit insight, the range of application in which TFET devices could bring a significant added value should be determined, considering today's processing capability, and future opportunities for aggressively scaled technologies

WP6 (leader: CCS)

N/A

WP7 (leader: LUND)

- WP 7 is dedicated to the dissemination and exploitation of the E^2SWITCH results. An E^2SWITCH logo and visual identity as well as the E^2SWITCH public website have been created. An E^2SWITCH flyer has been produced and a first E^2SWITCH press release has been launched. 38 E^2SWITCH dissemination activities (conferences and publications) have been carried out and a first E^2SWITCH public workshop has been held. An E^2SWITCH video introduction is in preparation. The E^2SWITCH exploitation strategy has been developed further and a technological roadmap has been proposed and refined.

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