Low power Tunnel FET circuits: challenges and opportunities

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Outline

• Technology scaling context
• Circuit design perspective
• System level opportunity
• Specialty component opportunity
• Summary
Future Application requirements

- **HIGH-PERFORMANCE COMPUTING**
  - Increased performance at constant power density
  - Constraints = Thermal and energy budget
  - Device: low-Vt, mobility boosters

- **HIGH-PERFORMANCE MOBILE**
  - Increased performance at constant leakage
  - Constraints = Battery, Leakage in multi-cores
  - Device: Strong SCE control
System scaling drivers = PPAC

- Node-to-node scaling targets
  - >50% area downscaling node-to-node
  - >30% more \textit{fmax} node-to-node at constant power
  - >20% more \textit{fmax} at constant leakage
  - >35% more \textit{fmax} at constant energy
  - <15% process cost

\textit{Pitch targets} – [nm]

\begin{tabular}{|c|c|c|c|c|}
\hline
Technology node – [nm] & 28 & 20 & 14 & 10 \\
\hline
CPP & 110 & 82 & 58 & 40 \\
MP & 90 & 64 & 44 & 30 \\
FP & 0 & 0 & 42 & 30 \\
\hline
\end{tabular}

CPP=Contacted Poly Pitch (Gate); MP=Metal 1 Pitch; FP=FinFET pitch
Scaling challenges?

No room for S/D contacts $\rightarrow$ high access resistance. But... this picture is not sufficient, better insight is required.
Technology roadmap

<table>
<thead>
<tr>
<th>V_{dd}</th>
<th>1.0-1.1V</th>
<th>0.9-1.0V</th>
<th>0.8-0.9V</th>
<th>0.7-0.8V</th>
<th>0.6-0.7V</th>
<th>0.5-0.6V</th>
<th>&lt; 0.5V</th>
</tr>
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</table>

- **Strain & Advanced Gate Stack Engineering**
  - SD/stressors
  - Metal Gate +High-k

- **Fully-depleted Channel for Improved Electrostatics**
  - Ultra-Thin SOI
  - Multi-gate FETs

- **Band-Engineered Channel for Enhanced Transport**
  - High-Mobility Channels
  - Nanowires/Tunnel FETs

- **Novel Materials/New Transport/Extreme Electrostatics**
  - 2D Materials
  - Quantum/Spin Devices
  - (Bi-layer Graphene)

**Tech Node**

- **32/28nm**
- **14nm**
- **7nm**
- **5nm**

**E2SWITCH**

- Feature Dimension & Voltage Scaling are concurrent drivers
- Material & Device Architecture Innovations Enablers of continual scaling
Technology roadmap

Full W/L variation

Width Quantization

Width / Length Quantization

Asymmetry

Design freedom

V_{dd}  1.0-1.1V  0.9-1.0V  0.8-0.9V  0.7-0.8V  0.6-0.7V  0.5-0.6V  < 0.5V
Electrostatic improvement not sustainable without new device architecture

CMOS Tech

Need “dramatic” electrostatic Scaling
Emerging device architecture

- TFET alternative architectures for so-called n5/n3 technology nodes

Circuit design perspective

- TFET for designer
- Logic cell design
- SRAM
Circuit design perspective - TFET

• Key Features
  – Band to Ban mechanism – Sub 60mv/Dec
  – Low VDD operation
  – Structure compatible with CMOS

• Challenges
  – Low Ion
  – Source engineering
  – Interface states

Device Expectation

- Logic properties
  - Steep SS
  - High drive
  - Low capacitance
  - Low Vt
  - Symmetrical device

- Model
Device Expectation

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- Model
TFET asymmetry

- **Unidirectional**
  - Forward FET device
  - Reverse - Diodes

- **Ambipolar**

  - **G - High**
    - **N-Type**
    - **D - High**

  - **G - Low**
    - **P-Type**
    - **D - High**
NAND gate design

- Shared source & Drains
- Source to drain connections
PLANAR CMOS NAND layout
PLANAR TFET NAND layout

Shared Node – How to deal with it?
TFET NAND layout

Extra area penalty (1 PP)
Increase metal congestion
What about vertical devices?

- Need to go from bottom to top
- Area penalty
SRAM

- Ambipolar behavior problematic for pass gates
- Special read/write scheme needed or other architectures

Cfr: Strangio et al. ESSDERC2014
Summary

• Uni-directionality forces update on layout template
• Might stress further the Lithography needs for logic
• In planar technology sharing nodes might be an option
System level opportunity

- High level analysis
- Activity factor 10% (10% of chip active)

System level opportunities for TFET in low speed context

Wei et al., VOL. 58, NO. 8, AUGUST 2011
Specialty component opportunity

Is their applications which would take benefit of extra TFET device in technology portfolio

- Internet of things
- High temperatures
- Analog applications
- Sensors
- RF
Summary

- TFET promised performances appealing for low power systems.
- Challenges in integration
- IP libraries must be updated
- Circuit topology and operation should take advantages of the TFET properties
Thank you &
Buon appetito