In the Quest of Zero Power: Energy Efficient Computing Devices and Circuits

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Abstract: This workshop is organized and supported by the E^2-SWITCH European Project (http://www.e2switch.org/) and will include a series of presentations dealing with state of the art advancements in Tunnel FETs as most promising energy efficient device candidates able to reduce the voltage supply of integrated circuits (ICs) below 0.25V and be hybridized with CMOS technology. The programme will also feature reports on DC/AC benchmarking for complementary n- and p-type Tunnel FETs, compact models for digital and analog/RF, device scalability, operational reliability and ITRS metrics.

8:50: **Introduction: the E^2-SWITCH project**, Adrian M. Ionescu, EPF Lausanne

9:00 Keynote 1: **Tunnel FETs: the promise and the reality**, Alan Seabaugh, University of Notre Dame, USA.

Biography:
Alan Seabaugh is a Professor of Electrical Engineering at the University of Notre Dame, Director of the SRC-NRI Midwest Institute for Nanoelectronics Discovery (MIND) and Associate Director of the Notre Dame Center for Nano Science and Technology. He received the Ph.D. degree in electrical engineering from the University of Virginia, Charlottesville, in 1985. Before joining the faculty at Notre Dame he held research positions at the National Bureau of Standards (1979 to 1986), Texas Instruments (1986 to 1997), and Raytheon (1997 to 1999). He has authored or coauthored more than 300 papers and over 90 invited presentations at conferences and workshops; he has 22 U.S. patents and 10 foreign patents and is an editor for the IEEE Transactions on Electron Devices. He received teaching awards in 1990 from U.T. Dallas and 2001 from Notre Dame. He was elected Senior Fellow at Raytheon in 1999 and IEEE Fellow in 2003. He received the Int. Symp. on Comp. Semicon. Quantum Devices Award in 2011 for seminal contributions and leadership in semiconductor devices and circuits based on quantum mechanical tunneling.

9:40 **SiGe strained nanowire tunnel FETs: integration and performance**, Qing-Tai Zhao, Siegfried Mantl, Peter Grünberg Institut-9-IT, Forschungszentrum Juelich, Germany.

10:05 **Simulation of Tunnel FETs for accurate performance prediction at device and circuit level**, Pierpaolo Palestri, Luca Selmi, DIEGM, Università degli Studi di Udine

10:30 **Coffee break**

11:00: Keynote 2: **Emerging Research Devices in ITRS: options for energy efficient computation**, An Chen, GLOBALFOUNDRIES, USA (*to be confirmed*)

Biography:
An Chen is with GLOBALFOUNDRIES, working on emerging logic and memory technologies. He is the Memory Technology Lead responsible for exploratory memory research with industrial consortia including IMEC and Sematech. His memory research focuses primarily on RRAM and STTRAM. Prior to GLOBALFOUNDRIES, he worked at Spansion LLC on emerging memory research and at Advanced Micro Devices (AMD) on nanoelectronics. He is currently chairing the Emerging Research Device (ERD) working group in the International Technology Roadmap of Semiconductors (ITRS). He is also a Senior Member of the IEEE.

11:40 **InAs/Si heterostructure tunnel FETs**, Kirsten Moselund, Heike Riel, IBM Zurich, Switzerland

12:05 **Low power Tunnel FET circuits: challenges and opportunities**, Morin Dehan, IMEC, Belgium (to be confirmed)

12:30-13:30: Buffet lunch

13:30 Keynote 3: **Benefits of SRAM design with tunnel FETs,** Costin Anghel, Andrei Vladimirescu, ISEP, France.

Biography:
Costin Anghel joined the research team at ISEP, Paris, France, in July 2008. He obtained his Ph.D. from Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland (1st European University and 15th Worldwide in Engineering/Technology and Computer Sciences, Shanghai ranking). After the Ph.D. he was employed as a project leader in the Electronics Laboratory, EPFL, Switzerland. In 2006 he obtained a Post-Doc fellowship at Commissariat à l'Énergie Atomique (CEA) LETI. During his Post-Doc he has worked mainly in the field of molecular electronics. His research interests include advanced devices like Tunnel Field Effect Transistors, organic/molecular devices, carbon nanotubes and their applications in electronics.

14:00 **Tunnel FETs for digital and analog/RF applications**, Lars-Erick Wernersson, University of Lund, Sweden

14:30 **Computing and sensing with steep-slope devices**, Adrian M. Ionescu, Nilay Dagtekin, Arnab Biswas, EPF Lausanne, Switzerland.

15:00 **End of Workshop**