E2SWITCH

Energy Efficient Tunnel FET Switches and Circuits

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SECOND PUBLISHABLE SUMMARY

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During its 2nd year, the E²SWITCH project made significant progress in terms of the advancement of SiGe/Si and InAs/Si complementary TFET platforms, the modeling and simulation platform and the benchmarking of both digital and analog figures of merit of TFET devices and circuits.

The main progress per WP is summarized in the following.

More information about the project can be found on the project website: www.e2switch.org/ The Output pages of the public website www.e2switch.org/output give an overview about all public project outcomes, namely publications, publishable summaries, workshops, an introductory video, press releases, and a flyer. Recent findings have been reported in our second workshop Steep Transistors Workshop - Energy Efficient Computing Devices and Circuits (5–6th October 2015, University of Notre Dame, USA - www.e2switch.org/output/workshops/*).*

WP1 TFET Device and Circuit Fabrication
Leader: JUELICH

JUELICH has fabricated successfully GAA Si nanowire complementary TFETs with suppressed ambipolarity, high on currents and minimum subthreshold swings <60mV/dec. The corresponding inverters show no longer a degradation in the voltage transfer curves (VTC), which is a considerable improvement compared to inverters with ambipolar C-TFETs. A novel SiGe/Si heterostructure TFET to exploit line tunneling was proposed (patent pending) and fabricated. Experimental results confirm that line tunneling increases the tunneling currents and improves the average slope. In matters of the novel GeSn semiconductor, for the first time negative differential resistance has been observed in GeSn p-i-n diodes, demonstrating band to band tunneling in GeSn p-i-n diodes.

IUNET-Udine has collaborated with JUELICH (with one young researcher of IUNET-Udine visiting JUELICH for 4 months) on the design of a half SRAM cell that should allow a comparison with the mixed device-circuit simulations of WP5.

IBM further developed the TASE growth technology, in particular the growth of vertical InAs NWs, TASE growth. IBM fabricated the first devices based on the lateral TASE technology. InAs MOSFETs and Hall-bars were used to validate the technology. The extracted high electron mobilities prove the excellent crystal quality of the achieved NWs. The process flow for the complementary TFET platform was established. Lateral InAs/Si p-channel TFETs were fabricated and characterized. A combination of scaled dimensions and improved gate and contact annealing resulted in good performance. IBM also fabricated the first InAs/GaSb tunnel diodes using the lateral TASE approach.

LUND has successfully fabricated InAs/GaSb vertical nanowire TFET devices with InAs diameters down to 11 nm.

WP2 Characterization
Leader: IBM

In WP2 we present the progress characterization of the various devices fabricated in WP1. Different characterization techniques are used for different devices, depending on their state of maturity.

DC and low-temperature measurements are done for TFETs from all three technology platforms: SiGe TFETs, InAs/Si TFETs and InAs/GaSb TFETs.

IBM reports on the first InAs/Si p-channel tunnel FETs implemented in the lateral TASE technology, these achieve high on-currents of about 8mA/mm at average slopes over several decades of current of about 70mV/dec, both at a 0.5V V_{DS} and 1V V_{GS} in the case of the I_{on}. Low temperature measurements are used to confirm TFET behavior, an I_{on} showing only a weak temperature dependence, combined with a relatively strong temperature dependence of the slope, caused by trap assisted tunneling.

IBM also demonstrated the first InAs/GaSb tunnel diodes implemented technology. Low temperature measurements show the impact of various physical mechanisms. Negative differential resistance (NDR) is visible even at room temperature.

LUND has focused their efforts on improving their vertical InAS/GaSb n-channel TFETs, in particular diameter scaling of the InAs part. They have reduced the subthreshold slope and increased I_{on} substantially as compared to their previously reported devices.

JUELICH has implemented the SiGe/Si TFETs with line tunneling, and investigated their low temperature characteristics. The results show improved tunneling transition from TAT to BTBT by using line tunneling. NDR was for the first time observed for the new material GeSn p-i-n diodes.

CV measurements are used to extract the interface trap density, D_{it}, and improve the gate stack.

JUELICH has investigated the influence of Sn concentration on the D_{it} in planar GeSn MOSCAPs.

LUND has carried out high-frequency characterization on arrays of vertical InAs NWs and worked on optimizing the InAs NW growth process to reduce D_{it}. LUND has also carried out CV measurements of the InAs/GaSb heterojunction in order to extract information on the heterojunction traps.

THE E2SWITCH CONSORTIUM

Ecole Polytechnique Fédérale de Lausanne
Lausanne, Switzerland

IBM Research GmbH
Zürich, Switzerland

Forschungszentrum Jülich
Jülich, Germany

University of Lund
Lund, Sweden

Eidgenössische Technische Hochschule Zürich
Zürich, Switzerland

IMEC Belgium
Leuven, Belgium

Cambridge CMOS Sensors
Cambridge, United Kingdom

SCIPROM Sàrl
St-Sulpice, Switzerland

Consorzio Nazionale Interuniversitario per la Nanoelettronica
Udine and Bologna

IBM has used CV characterization to evaluate the impact of various process steps in reducing D_{it} on both Si, InGaAs, InAs and GaSb planar MOSCAPs. In particular IBM has investigated the role of gate stack anneals, pre-deposition cleans and actual dielectric deposition conditions.

RF and Noise characterization has been carried out by LUND on arrays of vertical InAs/GaSb NWs. A a maximum cut-off frequency of f_t = 5.1 GHz has been achieved at V_{GS} =V_{DS}= 0.5 V. Noise is evaluated as a function of frequency.

Strain characterization. JUELICH has investigated the impact of growth conditions on the amount of strain in SiGeSn/GeSn/SiGeSn double heterostructures using XRD imaging.

IBM has carried out strain characterization, extending the set-up to enable simultaneous Raman/electrical/PLL measurements.

Characterization for compact model calibration. EPFL has characterized devices from JUELICH in terms of DC characteristics I_D-V_{GS}, g_m-V_{GS}, I_D-V_DS, g_{ds}-V_{DS} and C-V capacitance measurements, from room temperature to +125°C, in order to extract and calibrate an analog TFET model capable of predicting the device analog performance for benchmarking and full circuit simulations. The results obtained with the calibrated model are reported in WP4 and WP5.

CONTACTS

Scientific coordinator
Adrian Ionescu, EPF Lausanne
adrian.ionescu@epfl.ch

Project manager
Kirsten Leufgen, SCIPROM
kirsten.leufgen@sciprom.ch

WEBSITE

www.e2switch.org

WP3 Simulation and Modeling
Leader: ETHZ

Objectives of WP3 in the second year have been to develop models for Si/SiGe hetero-junction TFETs, to provide JUELICH with optimal design guidelines for TFET architectures with SiGe and GeSn/SiGeSn hetero-junctions, to provide IBM with design guidelines for all-III-V and Si/III-V hetero-junction nanowire TFETs including different strain configurations, to assess quantitatively the impact of non-ideal effects such as surface roughness, dissipative scattering, defects, traps, and localized charges on the nominal characteristics of TFETs, and to provide analytical expressions and compact models for TFET currents and capacitances backed up by TCAD simulations and by realistic assumptions about processes and layouts. All these objectives have been achieved.

The significant results of WP3 in the second year are: (1) Computed band structure quantities necessary to model BTBT in GeSn/SiGeSn hetero-junction TFETs based on derived empirical pseudopotential parameters for α-Sn. (2) In-depth study of the effect of conduction and valence band offsets on the sub-threshold swing of GeSn/SiGeSn hetero-junction TFETs. (3) Comparison of different TCAD calibrations for Ge- source TFETs showing that there is a complex interplay between direct and phonon-assisted tunneling when going from bulk materials towards aggressively scaled TFETs. (4) In-depth comparative simulation study of InAs/Si and All-III-V hetero tunnel FETs varying radius, equivalent oxide thickness, local doping, valence band offset, temperature, and trap-assisted tunneling parameters with focus on sub-threshold slope and on-current. (5) Deeper understanding of the impact of strain on band structure parameters and source/drain degeneracy level, which affect the sub-threshold slope, the leakage, as well as the on-state current. (6) Optimization of an n-type GaSb/InAs TFET exploiting biaxial tensile strain. (7) New TCAD models to include the effects of channel quantization and surface roughness on line tunneling in gate-overlapped-source TFETs. (8) New TCAD model to include the effect of random dopant fluctuations (RDF) on the sub-threshold swing of TFETs based on the description of RDF-induced DOS tails in the frame of trap-assisted tunneling. (9) Parasitics compact model for vertical TFETs which supports various materials and which is calibrated on TCAD for various geometries (e.g. different extension lengths and spacer thicknesses).

A new compact model for the analog simulation of TFET in Double-gate architecture implementations, based on an analytical closed form solution of 1D Poisson equation and using Kane's model for BTBT current calculations, including parameter calibration procedure, has been developed and implemented in Verilog-A This model is currently used in WP5 and WP6 for TFET circuit simulations and benchmarking, respectively.

WP4 Advanced Device Concepts for Sub-thermal Switching
Leader: EPFL

The work related to WP4 progressed according to the initial planning with contributions from partners EPFL, ETHZ, IUNET-Udine and IUNET-Bologna. Utilizing the simulation platforms developed in the first year of E²SWITCH, extensive simulations of Density-of-States (DOS) TFET switches using different dimensionalities were performed and the various resulting characteristics and performance metrics have been compared.

ETHZ, using OMEN, simulated a Si-InAs heterostructure TFET with various geometrical dimensions and noted the transition from 2D-2D to 3D-3D tunneling. The major highlight of the study is the trade-off between the ON current and the switching slope. 3D-3D tunneling provides higher ON current, at a cost of poorer switching slope performance.

EPFL, jointly with IUNET-Udine, performed extensive parameter variation simulations on the Electron Hole Bilayer TFET (EHBTFET). It is found out that, depending on the channel thickness and the channel material, the EHBTFET can either operate as a 2D-2D tunneling or a 3D-3D tunneling device. As the result of the exhaustive simulations using the EMA-NP code, III-V materials (InAs) seem to offer the highest performance both in terms of alignment voltage required and the ON current levels; mainly due to the low direct bandgap of InAs.

Moreover, EPFL proposed and validated (via 2D simulations) a novel approach to suppress the lateral leakage of the EHBTFET. The counter-doping approach was seen to very efficiently suppress the leakage, while preserving the ON current thereby allows EHBTFET to achieve a very impressive switching slope for several decades of current. EPFL also worked on the different biasing schemes for

EHBTFET and it is found out that using pseudo-bi-layer configurations (i.e. no charge is induced at the alignment point) is beneficial.

For the assessment of different dimensionalities, EPFL developed a modified version of the 2D code that incorporates quantization along the transverse direction. The code was then utilized to compare different dimensionality cases such as 2D-2D face vs. 1D-1D face tunneling.

By using Sband, IUNET-Udine calibrated the non-local dynamic path band-to-band tunneling model of the device simulator SDevice.

IUNET-Bologna has carried out a simulation study on the effect of strain on device performance with the aim of devise an optimum III-V heterojunction TFET. The conclusion is that biaxial tensile strain induces a remarkable ION enhancement, due to bandgap reduction and a more favorable band line-up at the heterojunction.

In conclusion, the work of WP4 permitted to screen the most promising DOS steep slope architectures where the dimensionality plays a major role but also to identify those that do not provide enough performance. All resulting solutions have been discussed with the project partners who lead the fabrication platforms. Their implementation raises big challenges in terms of adapting the existing SiGe/Si and InAs/Si platforms and further interactions continue in order to devise a proof-of-the concept path and/or set the basis for a future project focused uniquely on this type of device architectures.

WP5 TFET Circuits
Leader: IMEC

The key objective of WP5 is to perform a digital and analog/RF design and evaluate TFET compared to CMOS as a scaling option.

Task 5.1, which aims at illustrating a small circuit simulation of TFET devices, has shown calibration of TCAD against NEGF based simulation from WP3. TCAD is then used for mixed mode device/circuit simulations. Various circuits have been illustrated to show TFET feasibility including SRAM, level shifters, and full adder circuits. In task 5.3 basic analog circuits like current mirror have been fabricated using Schottky barrier (SB) MOSFET. Initial measurements are under way, which show very good output characteristics for the current mirror. Various different analog layout proposals have also been made for other key analog building blocks like common source circuits, cascade circuits etc. In Task 5.4 an initial calibrated TFET compact analog model has been made based on experimental data. This would allow performing design evaluation of usage of such TFETs in analog RF front end designs and will be further calibrated in year 3 on the optimized devices resulting from SiGe/Si and InAs/Si complementary platforms. Additional work is also under way in task 5.5 to build basic ground rules and standard cell architectures for vertical TFETs. Given vertical device pose an unique problem of not sharing source/drain escape electrodes are needed to access these terminals. Combination of Task 5.4, 5.5 and 3.5 would allow a complete analysis leaded by IMEC for digital circuits including all involved parasitics.

WP6 Digital and Analog/RF with emphasis on automotive
Lead: CCS

The work in WP6, developed along digital and analog/RF benchmarking from device to circuit level, made great progress in this reporting period.

IBM has evaluated appropriate ways of benchmarking published experimental TFET data, and carried out a benchmarking based on the average SS vs I_D/V_{DS}. In parallel, IMEC has reviewed the industrial technology roadmap for digital circuits and performed simulated benchmarking of the calibrated TFET device model in device level and digital AC figure of merits. In summary, the Energy and Delay of digital TFET are penalized by low I_{on} achievable and by larger capacitance due to longer gate length. Increasing the number of wires will not improve the performance further since it also increases the device capacitance, penalizing the speed gained with increasing the drive current.

We have established a systematic benchmarking study of analog figures of merit of 28nm sSi TFETs versus 28nm FD-SOI, CMOS based on a universal compact model at both device and circuit levels. Simulations showed very encouraging results, especially: (i) high TFET gain at very low current levels (1pA/mm to 10nA/mm), (ii) current gain cut-off frequency and unity gain frequency per unit power versus current shows significant performance

improvements below 10nA/mm. and (iii) a higher temperature stability for key analog IC functionality. For the first time using TFET device, we simulated transistor-connected diode using nTFET and pTFET devices where we have shown very high linearity from 0 to 200°C when compared with CMOS. Simulated results also show that when compared to TFET, $dV_D/dTemp$ does not change significantly with bias current variation. We also simulated and benchmarked a differential stage with TFET with active TFET load, biased with an ideal constant current source where the gain roll-off is significantly less compared to CMOS and this can be translated as improved energy efficiency offered by TFET circuits.

WP7 Dissemination and exploitation
Leader: LUND

The E²SWITCH WP7 is dedicated to the active and broad dissemination and exploitation of the results of E²SWITCH.

To this end, the E²SWITCH public website has been continuously updated and a statistical analysis of the site has been carried out.

The E²SWITCH plan for use and dissemination has been updated. We have increased the number of dissemination activities significantly. Overall, the E²SWITCH consortium has published 40 peer-reviewed articles, 52 scientific presentations and 10 other dissemination activities so far. The E²SWITCH exploitation strategy has been developed further and the technological roadmap has been refined.

Moreover, EPFL has submitted an application to the EC 2015 Innovation Award Competition resulting from STEEPER and E²SWITCH in terms of a novel image sensor using TFETs.

The networking activities have been particularly important during the International Workshop entitled "Steep Transistors Workshop" that was arranged on Oct 5-6, 2015, at the University of Notre Dame, USA. The workshop was co-organized by the E²SWITCH consortium and its US sister organization, LEAST (Low-Energy System Technology), by Prof. A. Seabaugh at University of Notre Dame and Prof. L.-E. Wernersson at Lund University, who also acts as Dissemination Manager for E²SWITCH. It was decided to host the workshop in the US to warrant a high participation from the US side as this increased the visibility in the US for the European effort. A mirror event will be organized in Europe by the end of the E²SWITCH project.