E2SWITCH Energy Efficient Tunnel FET Switches and Circuits

E^2SWITCH Project

Functional diversification with Tunnel FETs

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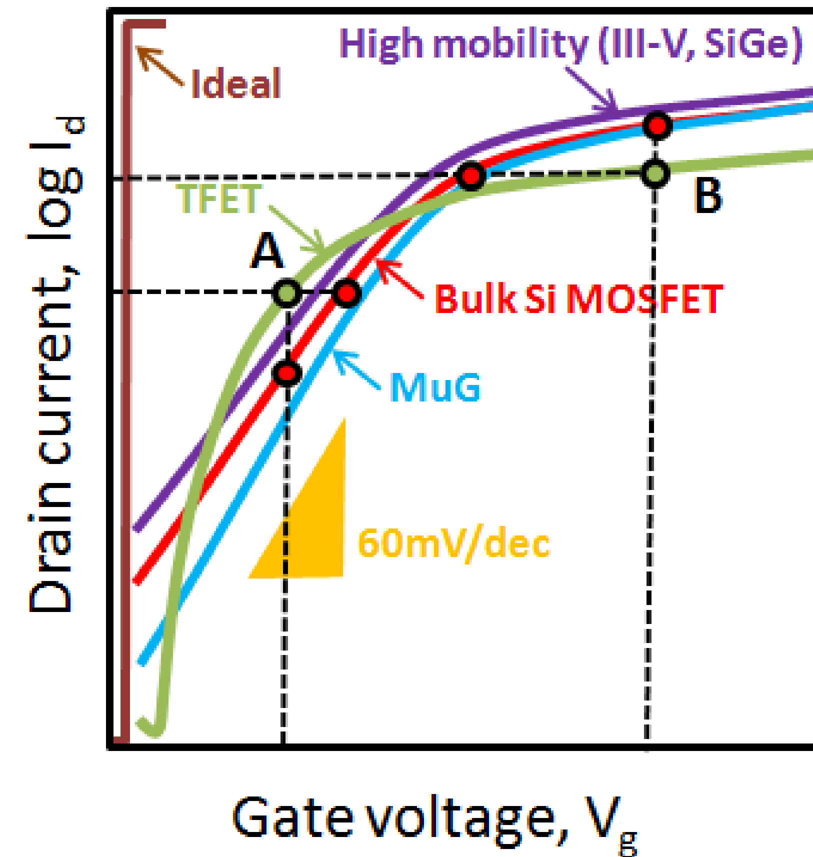
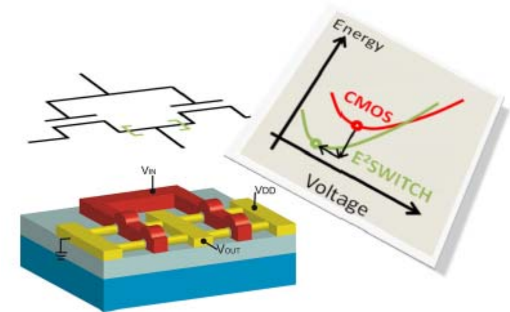
E^2SWITCH project

- Goals:
  - **Digital Tunnel FET**: operating at 0.25V with 10x better efficiency compared to nano-CMOS
  - **TFET fabrication** and technology optimization based on two advanced platforms
    - ✓ Complementary strained SiGe/Ge TFETs on silicon
    - ✓ Complementary III-V TFETs on silicon
  - **Analog Tunnel FET**: Exploration of new applications of Tunnel FETs in the field of analog/RF integrated circuits



E^2SWITCH partners



No	Name	Short name	Country
1	ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE	EPFL	Switzerland
2	IBM RESEARCH GMBH	IBM	Switzerland
3	FORSCHUNGSZENTRUM JUELICH GMBH	JUELICH	Germany
4	LUNDS UNIVERSITET	LUND	Sweden
5	EIDGENOESSISCHE TECHNISCHE HOCHSCHULE ZURICH	ETHZ	Switzerland
6	INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM VZW	IMEC	Belgium
7	CAMBRIDGE CMOS SENSORS LIMITED	CCS	United Kingdom
8	SCIPROM SARL	SCIPROM	Switzerland
9	CONSORZIO NAZIONALE INTERUNIVERSITARIO PER LA NANOELETTRONICA	IUNET	Italy

Analog Tunnel FET (1)

- Surface potential based **compact model** for all regimes of operation
- **Benchmarking** againts 28nm FD SOI MOSFET (STMicroelectronics)

EPFL: compact DC & AC ambipolar model

$$\varphi_S(x) = \varphi_S^0 + (V_D - V_S + 2V_{BI})\,\frac{\sinh\,(x/\lambda)}{\sinh\,(L_G/\lambda)} + \cdots$$

$$(V_S - V_{BI} - \varphi_S^0)\,\frac{\sinh\,(x/\lambda) + \sinh\,(L_G - x)/\lambda}{\sinh\,(L_G/\lambda)} \quad (1)$$

$$E_G(T) = (A - B(T^2/(T + C))) \quad (2)$$

$$t_{src}(T) = \kappa_C[CB(hQf + 3U_t)] - \kappa_V[VB(hQf + 3U_t)] \quad (3)$$

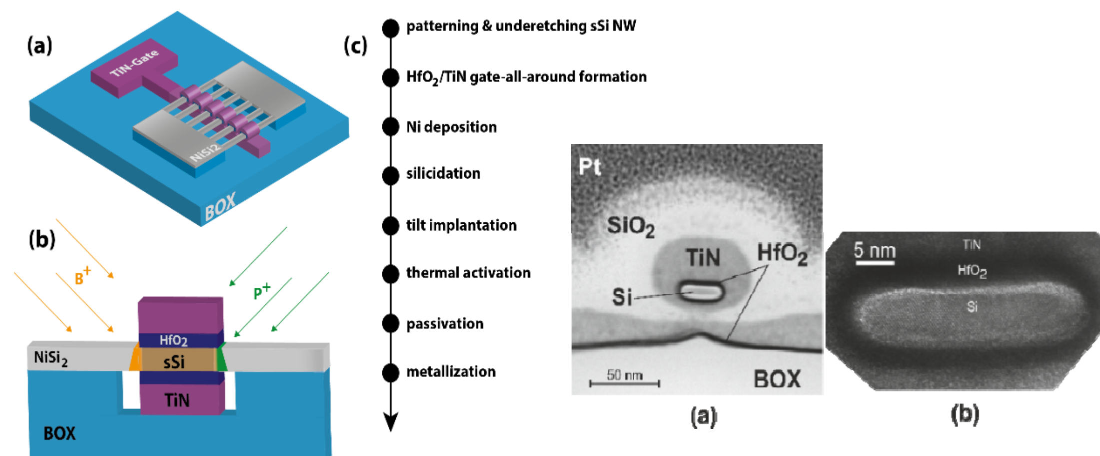
$$t_{drn}(T) = \kappa_C[CB(eQf - 3U_t)] - \kappa_V[VB(eQf - 3U_t)] \quad (4)$$

$$G_{src} = A_{pat\,h}(T)\left[\frac{E_G}{t_{src}}\right]^P exp\left(\frac{-B_{pat\,h}(T)t_{src}}{E_G}\right) \quad (5)$$

$$G_{drn} = A_{pat\,h}(T)\left[\frac{E_G}{t_{drn}}\right]^P exp\left(\frac{-B_{pat\,h}(T)t_{drn}}{E_G}\right) \quad (6)$$

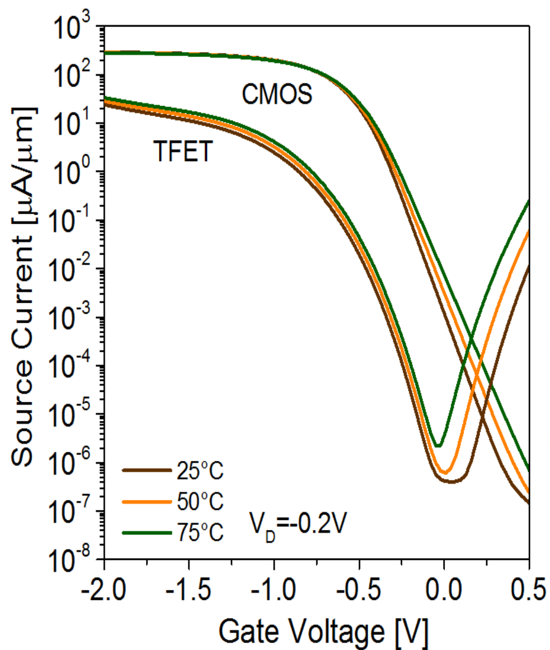
$$I_{tunn}(x,T) = qW_{ch}t_{ch}(G_{src} + G_{drn}) \quad (7)$$

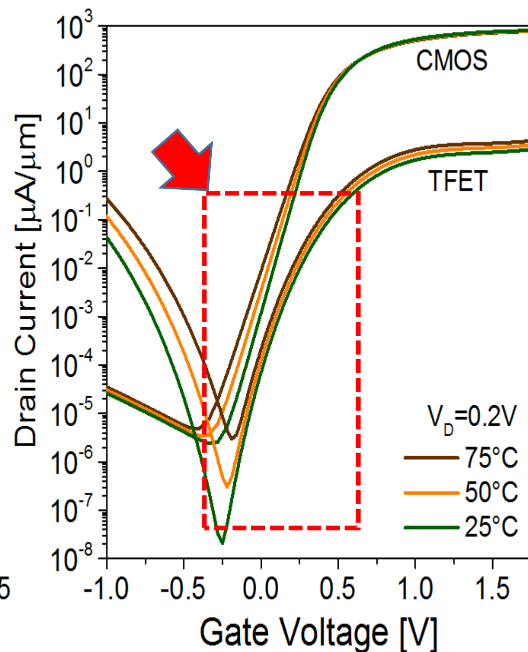
Juelich: Complementary sSi Tunnel FETs

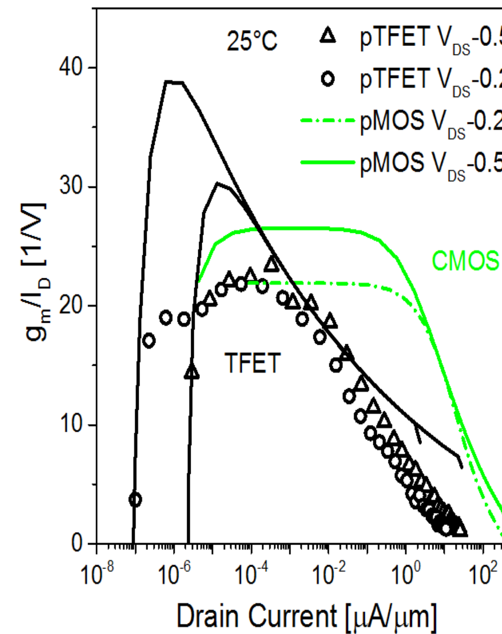


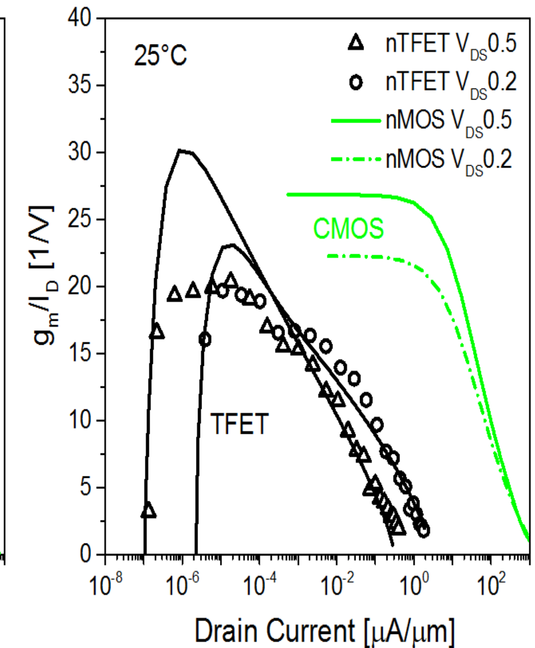
Analog Tunnel FET (2)

- 28nm Complementary Tunnel FETs versus FDSOI CMOS: benchmarking
- High analog gain and unity gain frequency per unit power for Tunnel FETs









1T APS with Tunnel FET

With 1 Tunnel FET:

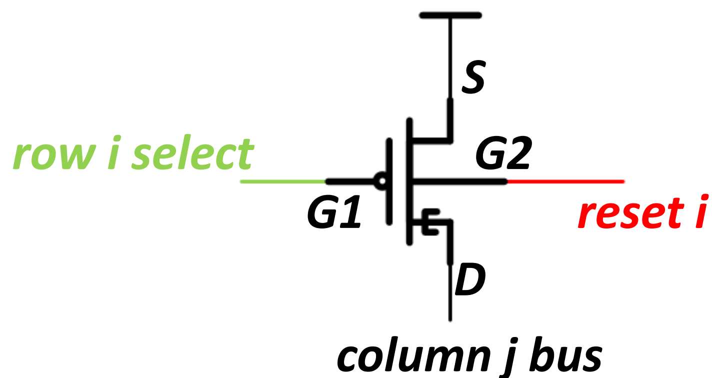
- light-charge conversion
- charge storage
- pixel operations (reset, cell selection)
- in-pixel amplification

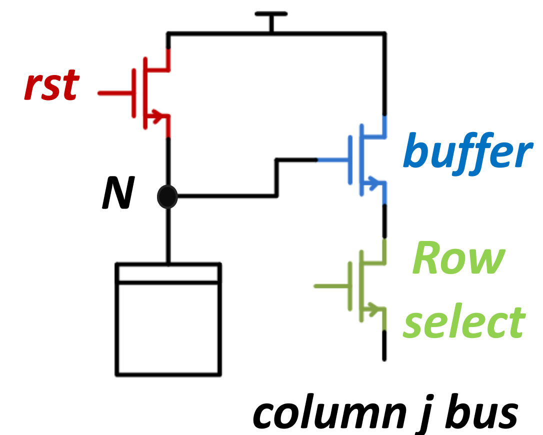
With CMOS:

Reset: reset is ON → "N" is initialized

Integration: I_P discharges "N"

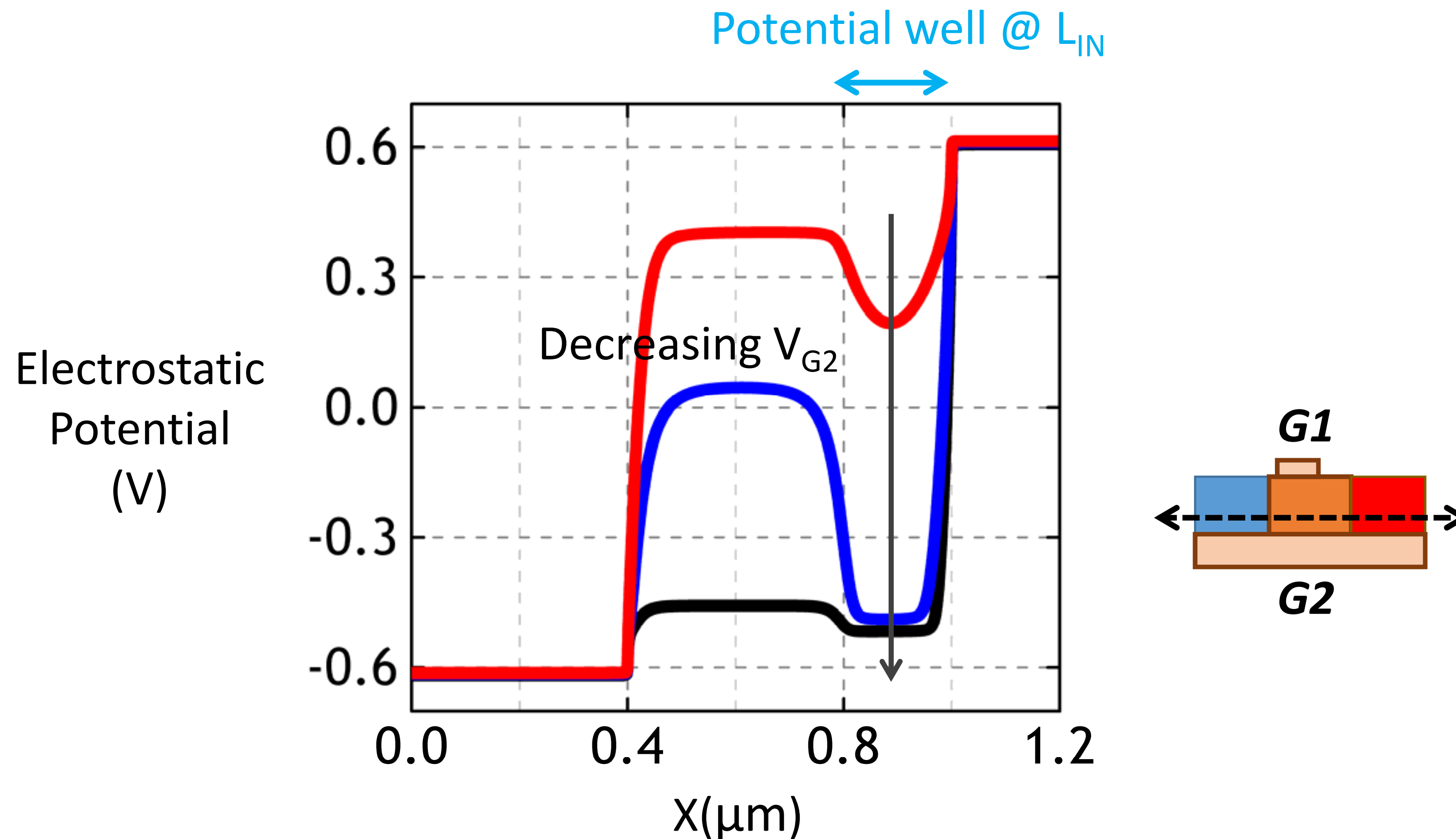
Read-out: row select is ON →column select





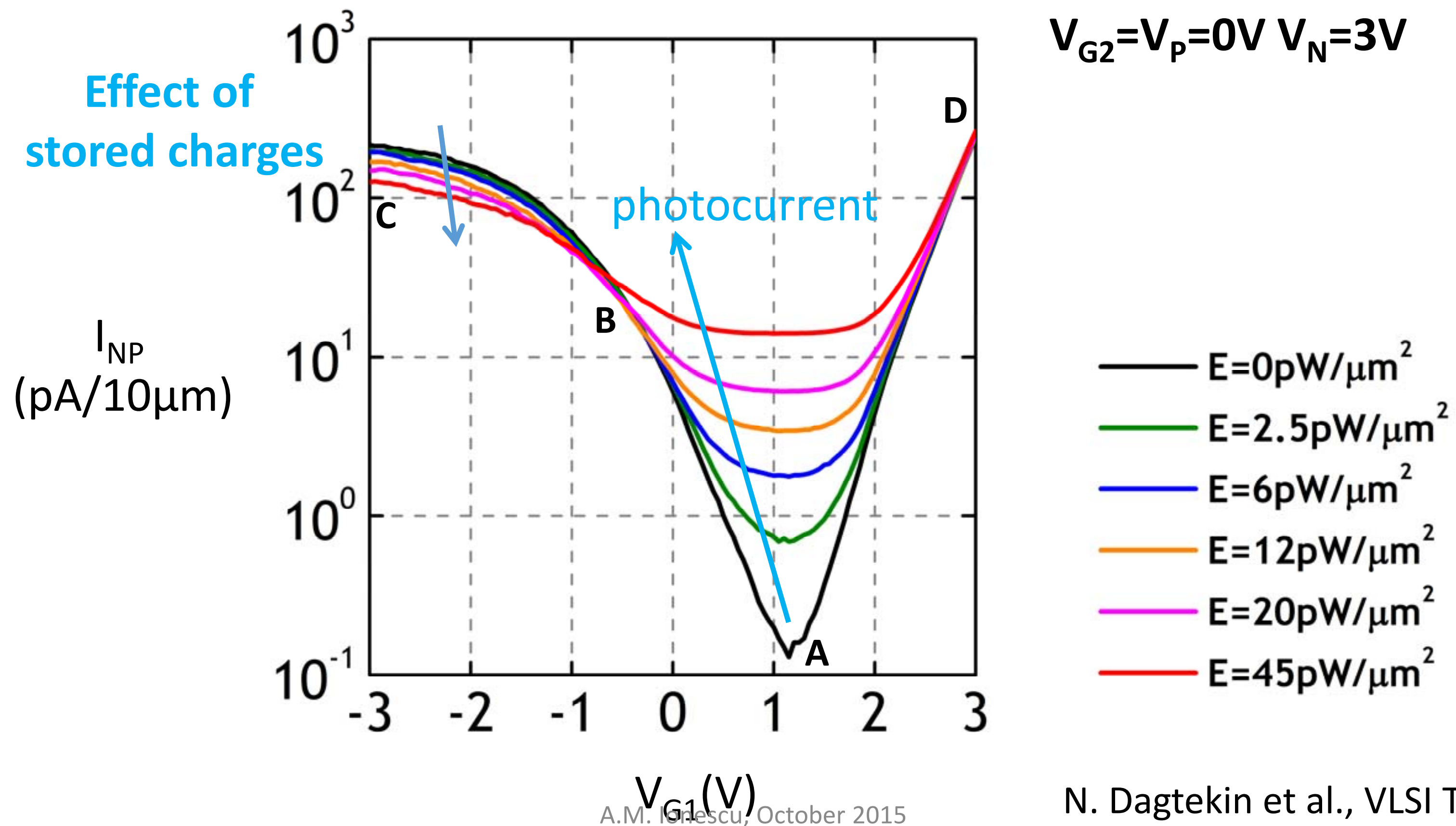
Tunnel FET with partial gate ovrlap

Charge storage, impact on tunneling current.



A. Biswas et al., APL, 2014

1 Tunnel FET APS



N. Dagtekin et al., VLSI Techn. Symp. 2015.

Functional diversification

- **Future analog and sensing functions with tunnel FETs**
  - ✓ @ very low current & voltage
  - ✓ analog gain @ very low current (sub-10nA)
  - ✓ steep slope: higher sensitivity for bio and gas sensors. Selectivity?
  - ✓ stability over larger temperature operation range
  - ✓ New image sensors
  - ✓ Energy efficient IoT applications