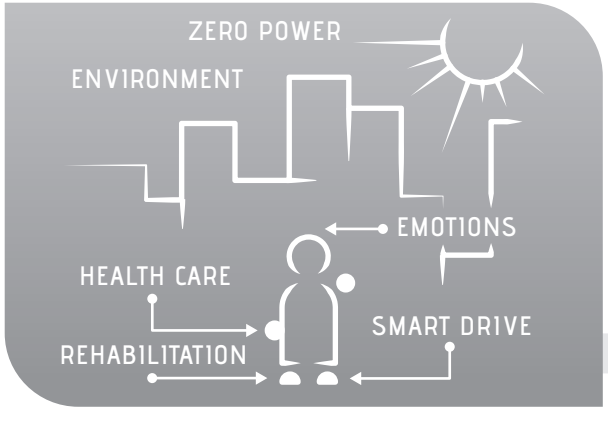
E²SWITCH

Energy Efficient Tunnel FET Switches and Circuits

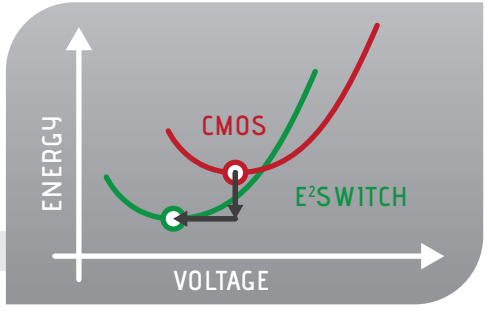
The consumption of electrical energy is steadily increasing and measures for power reduction will be required. Low-power devices are basic building blocks for any circuit. They must operate at the lowest achievable power consumption in stand-by mode as well as during operation. An extremely low supply voltage combined with negligible off-current are essential for reducing power consumption. We aim at > 10 times power reduction by the use of novel devices.



MISSION AND VISION

E²SWITCH focuses on Tunnel FET (TFETs) as most promising energy efficient device candidates able to reduce the voltage supply of integrated circuits (ICs) below 0.25V and make them significantly more energy efficient by exploiting strained SiGe/Ge and III-V platforms, with CMOS technological compatibility.

A full optimization and DC/AC benchmarking for complementary n- and p-type TFETs, integrated on the same fabrication platform, is proposed. Compact models are developed and implemented in Verilog A, for portability, to support the design of low power ICs with CMOS architectural compatibility for: (i) digital and (ii) analog/RF.



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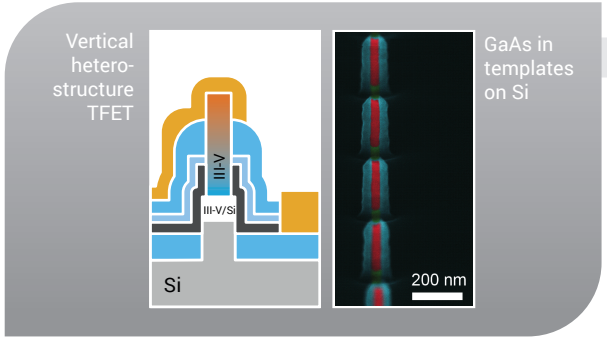
IMEC Belgium
Cambridge CMOS Sensors
SCIPROM Sàrl
Consorzio Nazionale Interuniversitario per la Nanoelettronica

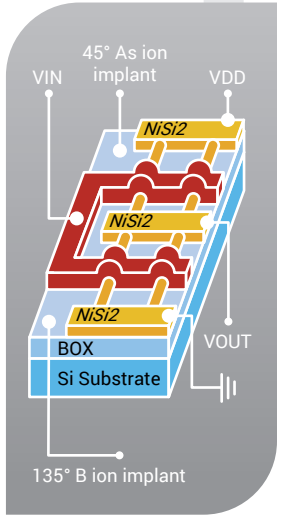
The E²SWITCH Consortium gathers nine organisations from a total of six different countries. Together they form a unique multidisciplinary network of universities, one large industrial partner, two research centres and one research-intensive SME, supported by a dedicated management SME.

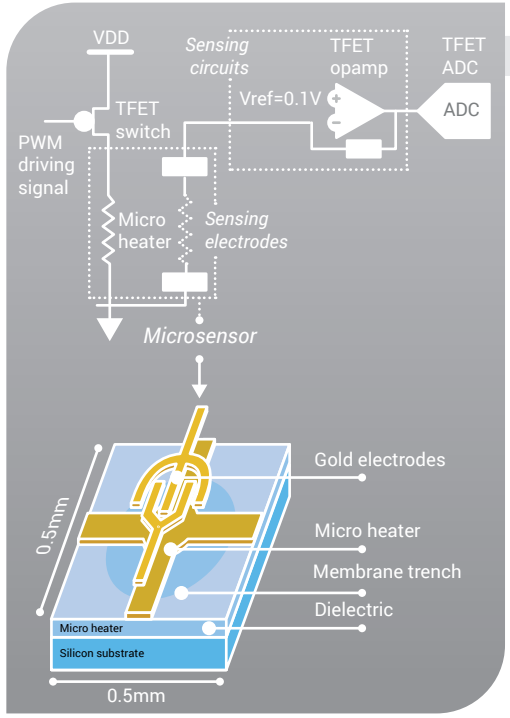
IMPLEMENTATION

III-V heterojunction TFETs and integration on a silicon platform using selective epitaxy in templates.



Investigation of complementary, scaled Si-based nanowire TFETs with wrapped around high-k/metal gates targeting on currents >100 µA/µm and minimum slopes <60 mV/dec.



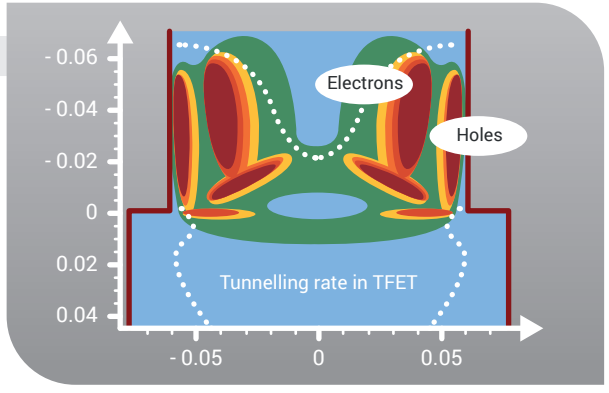


MISSION AND VISION

Within the scope of the project our aim is to exploit TFET solution for energy efficient, ultra-low power and low voltage, System-On-Chip for portable sensing applications, such as smartphone and wearable sensors for health and well-being. Initially, we will be benchmarking simple TFET analog front end building blocks vs CMOS circuitry to determine optimal solution for driving micro-heaters and sensing circuits.

THEORY

Computer-aided design of TFETs by predictive multi-scale device simulation.



Mixed device/circuit simulations of basic building blocks of analog and digital systems.